Anirudha Behera

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EDUCATION

Illinois Institute of Technology, Chicago, USA **12/2023**
Master of Science in Electrical Engineering, **GPA 3.53/4.0**
Relevant Coursework: Introduction to VLSI, CAD Techniques for VLSI Design, High-Performance VLSI/IC Systems, Digital SoC Design, Computer Organization and Design, RF Integrated Circuit Design

Gandhi Institute For Technology, Bhubaneswar, India **07/2018**
Bachelor of Technology **in** Electrical Engineering, **GPA: 8.1/10**

SKILLS

Scripting/Programming Skills: TCL, Perl, Shell Scripting, Python, VHDL, Verilog
EDA Tools: Synopsys (IC Compiler II, Design Compiler, PrimeTime, Star RC, IC Validator, Hspice, Formality), Cadence (Virtuoso, Encounter), MG/Siemens (Calibre, ModelSim), Xilinx Vivado, CACTI, WATCH, Redhawk
Interpersonal Skills: Project Deadline management, communication skills, multitasking, leadership, quick learning.

WORK EXPERIENCE

Research Assistant, Design Automation LAB, IIT, Chicago, USA **08/2023 - 12/2023**

- Advisor: Dr. Ken Choi, Professor, ECE Department, IIT Chicago.
- Implemented RTL to GDSII flow for 14nm and 28nm TSMC technology nodes on block-level JBI processor using Synopsys tools.
- Analyzed operating condition variations across design using MCMM and RC corner cases.
- Developed a novel methodology by combining Floorplan and Power plan in one stage for optimizing runtime and QOR.
- Research Article: Precision Methodology: Transforming VLSI Physical Design with Tailored Floorplan and Power Plan Strategies.

Physical Design Intern, Chipedge Technology, Remote **10/2022 - 07/2023**

- Led end-to-end Physical design phases, Logic Synthesis, Floorplan, Placement, Clock Tree Synthesis (CTS), Routing and Optimization. monitored Quality of Results (QOR) against Power, Performance, and Area (PPA).
- Analyzed Timing/SDC constraints and resolved STA violations through holistic strategies for designs with up to 10 million standard cell instances and over 80 macros across 14nm, 22nm, 32nm and 45nm FinFET/CMOS technology nodes from TSMC.
- Ensured design integrity during Sign-off by extracting parasitic elements (.spef) and progressively resolving DRC, LVS, EM/IR, and LEC issues.
- Employed ECO cycles and extensive manual debugging techniques for successful GDSII tape-out.
- Utilizing Shell and TCL scripting across Physical Design methodology from RTL to GDSII.

ACADEMIC PROJECTS

OpenSPARC T1 Block Level design from RTL to GDSII using 14nm and 28nm TSMC nodes | DC | ICC2 **01/2023**

- Used 75% core-area utilization and density sweeps to understand the congestion and routability behavior.
- Optimized design using insertion and size cell techniques to eliminate DRV's like Caps and Trans.

Standard Cell-Based 32-bit Pipelined CPU Design with Modified New ALU Architecture (RTL to GDSII) **11/2022**

- Implemented 5 different CPU models with ASIC flow for slack time optimization.
- Executed Synthesis, PNR, and Opt then recorded optimized slack time, power, area and Obtained GDSII Layout.
- Utilized CSeA, CLA, CRA and CSA adders and comparator-CLA mix designs and compared their performance.

CAD Tool Design for Static Timing Analysis by using TCL/Tk and C Programming **11/2022**

- Designed C code to calculate the required time, arrival time, and slack time from the given input vectors and optimized the code to save the output file separately.
- Designed a Static Timing Analysis CAD tool GUI using TCL/Tk, which can take set of inputs from the user and optimize the given input vector using implemented C code and display the output results on the GUI interface.

Multimedia Mobile Processor Configuration for Ultra-low Power Design | WATCH | CACTI | ModelSim **04/2023**

- System-Level: Coded Graph-based slack analysis in C. Optimized with Loop unrolling and catch technique. WATCH and CACTI tools were used. Achieved 85.68% power reduction.
- RTL-Level: Applied ACG, CCG, OCCG, LECG, ECG, hybrid techniques on MMP. Achieved max 109.75% power reduction. Used Formality, Model Sim, Power Compiler (DC) tools.

LEADERSHIP: Secretary General at Eta Kappa Nu Delta Chapter HKN-IEEE Government, IIT-ECE Dept. **01/2023**